The possibility of giant dielectric materials for multilayer ceramic capacitors

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There have been numerous reports on discovery of giant dielectric permittivity materials called internal barrier layer capacitor in the recent years. We took particular note of one of such materials, i.e., $BaTiO_3$ with SiO_2 coating. It shows expressions of giant electric permittivity when processed by spark plasma sintering. So we evaluated various electrical characteristics of this material to find out whether it is applicable to multilayer ceramic capacitors. Our evaluation revealed that the isolated surface structure is the sole cause of expressions of giant dielectric permittivity. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4791555]

Demand for multilayer ceramic capacitors of smaller size and higher capacitance is ever increasing as electronic devices, such as digital home appliances, PCs, and mobile phones get smaller, thinner, and multi-functional. In order to satisfy such needs, we need to use a higher electrical permittivity material or increase the number of dielectric thin-film layers.

As an example, let us suppose we design a multilayer ceramic capacitor of 10 μF of size 0.6 mm × 0.3 mm × 0.3 mm that will probably become one of our main products in the near future. If we design C0603-106 using $BaTiO_3$ (BT) whose electrical permittivity is 1500, we would probably have to laminate about 1000 dielectric and internal electrode layers whose thickness would be 0.15 μm, respectively. If the BT grain size is less than 100 nm, it cannot keep high electrical permittivity because electrical permittivity deteriorates as a result of significant deterioration in crystal forms and anisotropic characteristics.[1,2] So it is difficult to increase electrical permittivity to 1500 if we use 50 to 100 nm grains even if we are successful in laminating 1000 or so layers.

On the other hand, there have been numerous reports on discovery of giant electric permittivity materials called internal barrier layer capacitor. For example, it is reported that $CaCu_3Ti_4O_{12}$, whose structure is similar to the perovskite structure, shows expressions of giant electrical permittivity.[3,4] According to Chung's reports, the sintering of BT coated with 5 nm SiO_2 by spark plasma sintering has produced about 130 000 electrical permittivity and 5% dielectric loss at room temperature.[5–7] Chung's experiments conducted under the vacuum condition revealed that the BT became oxygen deficient and semiconductive, turning the SiO_2 coating layer into an insulating layer. We thought as Chung did that the structure became that of the internal barrier layer semiconductor ceramics. However, electrical permittivity of SiO_2 is about four. That means electrical permittivity of enormous 130 000 is not computationally attainable, so it must be just a superficial or apparent relative dielectric permittivity. So we guessed that there are some other unknown effects, for example, interface materials or improvement of the dielectric constant brought about as a result of strain.

If we could use this kind of giant dielectric permittivity material instead of BT, it should be easy to design much smaller multilayer ceramic capacitors having higher capacitance. Unfortunately, only a few papers discuss electric characteristics from the perspective of practical implementation of this effect. So we made extensive studies in order to determine whether this kind of giant permittivity material can be used in actual multilayer ceramic capacitor design. Concretely speaking, we coated the BT grains of about 500 nm coated with a 5 nm thick SiO_2 layer in the same manner as what is described in Chung's reports, sintered them by spark plasma sintering, and evaluated various electrical characteristics.

We prepared BT grains of about 500 nm diameter coated with 5 nm thick SiO_2 by the Stober method (hereinafter referred to as BT500@Si5).[8] We then made a composition analysis by ICP-AES (Shimadzu ICPS-8100CL) to make sure that the amount of coated SiO_2 is equal to the amount charged. Coating quality was confirmed by TEM observation (JEOL JEM-2100F).

1 g of BT500@Si5 powder was charged into a φ 12 mm graphite mold of SPS-515 S (Sumitomo Coal Mining Co, Ltd). In a vacuum ambient (about 5 Pa), temperature was raised to 1175 °C at a rate of 100 °C/min with 50 MPa pressure on longitudinal uniaxial direction. The temperature was kept there for 3 min. The disk obtained was then kept in an atmosphere of 800 °C for 12 h in order to compensate for oxygen vacancy and remove contamination of graphite. After completion of the second round of this process, the disk was then kept in an atmosphere of 900 °C for 12 h.

We made electrodes on the disk by applying paste of In-Ga eutectic alloy to the disk surface. We measured the temperature characteristics of capacitance and dielectric loss of the disk. Using AMQ-064-C (Espec Co, Ltd), we supplied 1 V rms signal and measured data varying frequency from 100 Hz to 1 MHz and temperature from −55 °C to 150 °C. Temperature characteristics of resistivity were measured with R8340 Ultra High Resistance Meter (ADVANTEST Co, Ltd) under the following conditions: applied voltage 1 V, measurement time 30 s, temperature range from 20 °C to 160 °C. Voltage-current characteristics were measured with Keithley237 High Voltage Source Measure Unit (Toyo corp.). AC impedance was measured with Solartron SI 1260

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(Toyo corp.) at room temperature over the frequency range from 1 mHz to 1 MHz.

We used JEM-2200FS (JEOL Co, Ltd) together with a scanning transmission electron microscopy-energy dispersive spectroscopy (STEM-EDS) detector to obtain a Si elemental mapping image in order to find out where Si exists.

We only confirmed existence of just 10% of the amount of SiO_2 charged even though we made the BT500@Si5 powder by following Mornet's coating method.[8] After dripping tetraethoxysilane (TEOS) in the slurry of BT and stirring, the pH was 7, so we thought that the amount of base that serves a catalyst of hydrolysis reaction of TEOS was not enough. So, we increased the amount of ammonia, a base, to accelerate the hydrolytic reaction of TEOS. As a result, the pH increased to 8.8, so we confirmed that the amount of SiO_2 was nearly the same as the amount charged. A TEM image of the BT500@Si5 powder made in the manner described above is shown in Fig. 1. Though the SiO_2 coating thickness is somewhat uneven, it shows that the BT grains are coated with SiO_2.

Then, the BT500@Si5 powder was sintered by spark plasma sintering. It was sintered twice in an atmosphere of 800 °C in the same manner as what is described in Chung's report in order to remove contamination of carbon used for releasing the disk from the mold and to compensate for oxygen vacancy caused by vacuum sintering. As a result, we obtained a bluish disk of 99% relative density. We measured the resistivity of the disk sintered twice at 800 °C. The result was $7 \times 10^4\ \Omega \cdot$cm. Chung's report does not mention any data of resistivity. We believe it must have been this low. We thought the reason for such low resistivity was because the reoxidation process at 800 °C did not quite take effect to fully compensate for oxygen vacancy. Multilayer ceramic capacitor practically needs more than $10^8\ \Omega \cdot$cm of resistivity. So we sintered the disk again in an atmosphere of 900 °C to promote further compensation for oxygen vacancy. Then, we got resistivity of higher than $10^9 \Omega \cdot$cm at room temperature, so we judged that oxygen vacancy was fully compensated at 900 °C. Results of evaluation of various electrical characteristics of the disk sintered at 900 °C are shown below.

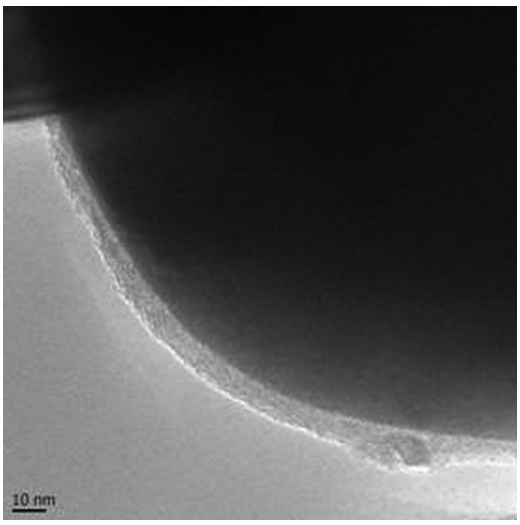

FIG. 1. TEM micrograph of BT coated with SiO_2.

Fig. 2 shows temperature dependency of resistivity in the range from 20 °C to 160 °C. It shows resistivity higher than $10^9\ \Omega \cdot$cm in the measurement range. Fig. 3(a) shows temperature dependency of dielectric permittivity in the range from −55 °C to 150 °C measured at different frequencies. Fig. 3(b) shows temperature dependency of dielectric loss in the range from −55 °C to 150 °C measured at different frequencies. The 10 kHz curve shows dielectric permittivity of 75 000 and dielectric loss of 21% at 25 °C with a peak near 130 °C. Dielectric permittivity is 113 000 at 100 Hz, whereas it is 13 000 at 1 MHz. Fig. 4 shows a curve of current-voltage characteristics. It shows no-ohmic characteristics and the varistor voltage was 0.23 V/μm based on 1 mA.

We thought that the sintered disk has the semiconductor ceramics structure of internal barrier layer, isolated by SiO_2. Then, it means SiO_2 determines the temperature characteristics. Because SiO_2 is a paraelectric, dielectric permittivity must be flat over the temperature range. But the result was different. In order to find out the location of SiO_2, we performed an Si elemental mapping of disk cross section by STEM-EDS (Fig. 5). We found no Si elements in the grain boundary of BT, but found it was segregated. And more, a point analysis by STEM-EDS detected almost no Si element in the substance existing between grain boundaries. This tells us that Si plays no important role of insulation because it cannot stay on the surface of grains. Rather, it diffuses during the sintering process. The peak near 130 °C indicates that tetragonal BT dominates the temperature characteristics. We presume the peak near 130 °C is the curie point. Chung's report also shows a peak near 130 °C. So our results agree with Chung's.

AC impedance of the disk sintered by spark plasma sintering was measured to figure out the structure of the semiconductor layer and the insulating layer. Results are shown in Fig. 6. In general, a circular arc appears if the real part and the imaginary part of the impedance are plotted on the complex plain. Fig. 6 shows a partial circular arc. It is because the disk still had high resistance at 160 °C. Based on an equivalent circuit that has both a semiconductor layer of BT with oxygen vacancy and an insulating layer of BT with compensated oxygen vacancy, we estimate that the semiconductor layer is 20 Ω, and the insulating layer is $10^{12}\ \Omega$. We measured the resistivity of the disk after polishing the

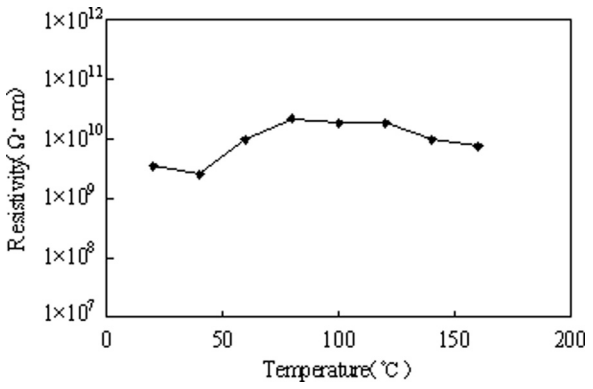

FIG. 2. Temperature dependence of resistivity of the disk sintered by spark plasma sintering.

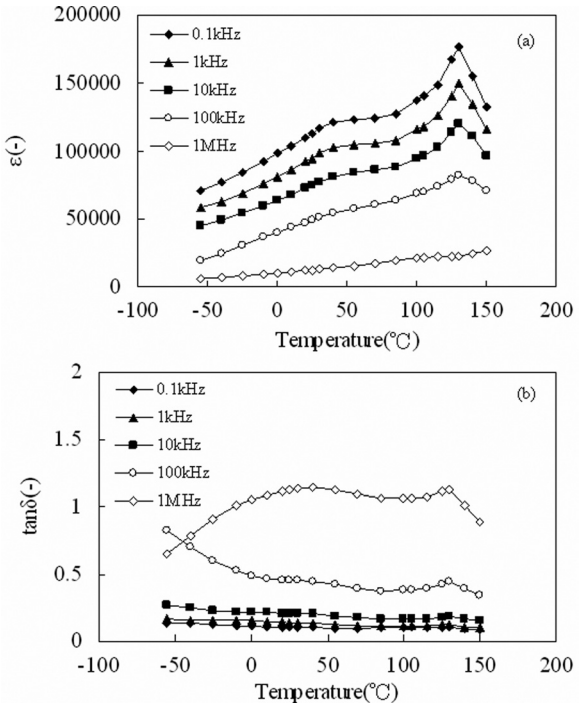

FIG. 3. (a) Temperature dependence of dielectric permittivity of the disk sintered by spark plasma sintering. (b) Temperature dependence of dielectric loss of the disk sintered by spark plasma sintering.

surface by about 130 μm to judge if the disk is an internal barrier layer type or an isolated surface type semiconductor capacitor. Resistivity measured less than several tens of $\Omega \cdot$cm, which is lower by 10^8 $\Omega \cdot$cm as compared with the value before polishing. From this result, we figured out that the disk has an isolated surface semiconductor structure and has a high resistivity layer only in the neighborhood of the surface.

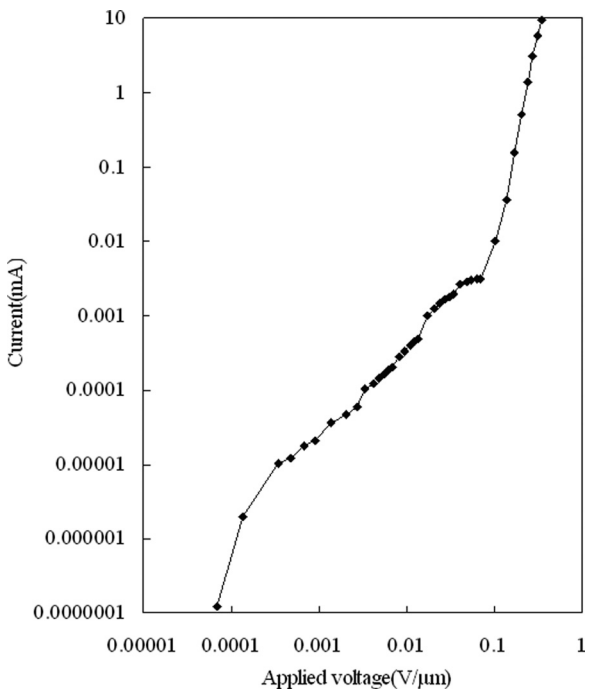

FIG. 4. The correlation curve of current and voltage of the disk sintered by spark plasma sintering.

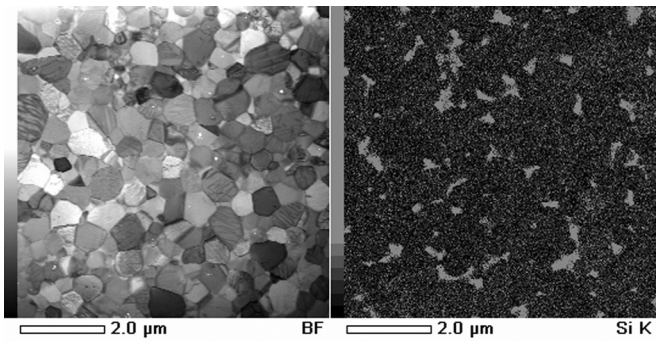

FIG. 5. Si mapping image of the interior of the disk sintered by spark plasma sintering (Left figure: bright field image and Right figure: Si mapping image).

According to Chung's reports, he observed dielectric permittivity of 130 000 and dielectric loss of 5%. But our data of dielectric permittivity is lower and our data of dielectric loss are greater as compared with Chung's data. The difference can be explained by the characteristics of our disk. That is, it has an isolated surface semiconductor structure and, therefore, is much more dependent on the disk shape. For example, relative dielectric permittivity becomes higher as the disk gets thicker, or so it appears. It is because the thickness of the semiconductor layer gets larger than that of the insulating layer as the disk gets thicker.

Meanwhile, we verified dielectric loss by a simulation using equivalent circuit. Fig. 7 shows a two-layer model whose capacitance and resistivity of the semiconductor layer and the insulating layer are C_1, R_1 and C_2, R_2, respectively, where C_2 is much higher than C_1 and R_2 is much higher than R_1. Formulas (1) below describe the real and imaginary parts of synthetic capacity C of the equivalent circuit.

$$C'(\omega) = \frac{\tau_1 R_1 + \tau_2 R_2 + \omega^2 \tau_1 \tau_2 (\tau_1 R_2 + \tau_2 R_1)}{(R_1 + R_2)^2 + \omega^2 (\tau_1 R_2 + \tau_2 R_1)^2}$$
$$C''(\omega) = \frac{R_1 + R_2 + \omega^2 (\tau_1{}^2 R_2 + \tau_2{}^2 R_1)}{\omega (R_1 + R_2)^2 + \omega^3 (\tau_1 R_2 + \tau_2 R_1)^2}, \quad (1)$$

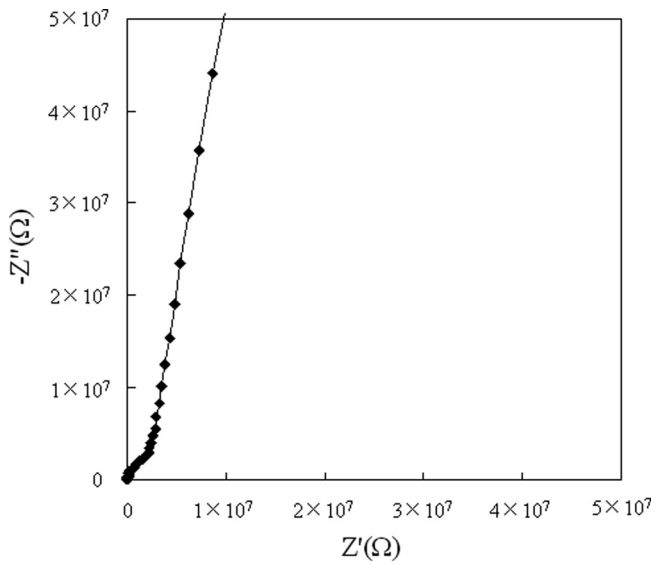

FIG. 6. AC impedance of the disk sintered by spark plasma sintering.

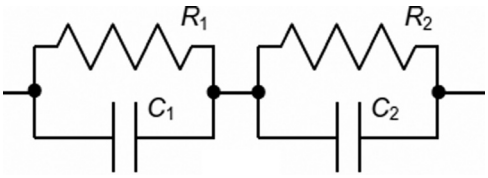

FIG. 7. A circuit representing the two-layer model.

where $\tau_1 = R_1C_1$ and $\tau_2 = R_2C_2$.

Dielectric loss is given in formula (2)

$$\tan\delta = \frac{C''(\omega)}{C'(\omega)}. \tag{2}$$

If plotted in a graph whose horizontal axis represents frequency (ω) and vertical axis represents dielectric loss ($\tan\delta$), resulting curve has a peak at a certain frequency.

$$\frac{1}{\omega} = C_1R_1. \tag{3}$$

As formula (3) indicates, the value C_1R_1 must be small to avoid relaxation at low frequencies. That means we need to keep resistivity of the semiconductor layer as low as possible. This analysis leads us to presume that resistivity of the semiconductor layer of our disk is higher than that of Chung's disk. We conducted a simulation experiment of Mornet's coating method employed by Chung. It generated only 10% of the total SiO_2 charged. So, we find it possible that the actual amount of SiO_2 of Chung's disk was lower than we thought and that is why apparent relative dielectric permittivity was measured high.

Finally, let us consider applying this material to multilayer ceramic capacitors. The varistor voltage was 0.23 V/μm based on 1 mA. Considering practical use of multilayer ceramic capacitors, the varistor voltage has to be at least 10 V/μm. But actually the voltage is way too low because it has a semiconductor capacitor structure. Double Schottky barrier φ is given by formula (4), which is obtained by solving the Poisson equation.[9]

$$\varphi = \frac{{Q_{GB0}}^2}{8q\varepsilon_s N_d}, \tag{4}$$

where Q_{GB0} is charge density captured by grain level. Q_{GB} is given by formula (5).

$$Q_{GB} = 2qN_dl_0, \tag{5}$$

where ε_s is dielectric permittivity near the grain boundary, N_d is donor density, q is charge, and l_0 is the thickness of the space charge layer. This formula tells us that the height of double Schottky barrier changes as dielectric permittivity near the grain boundary changes. Raise the height of double Schottky barrier to raise the varistor voltage and dielectric permittivity conversely decreases.

Let us consider designing a C0603-10 μF capacitor using this material. For example, if the thickness of the dielectric layer and the internal electrode layer is 1 μm, respectively, required apparent relative dielectric permittivity and the number of layers would be 59 000 and 145, respectively. The insulating layer of BT whose oxygen vacancy is compensated must be as thin as 25 nm if its dielectric permittivity is 1500. With that thickness, there will be no good insulating properties. It leads us to believe it is not viable to use this material for multilayer ceramic capacitors. Capacitors of isolated surface semiconductor type show high apparent relative dielectric permittivity. However, this type of capacitor is dependent on structure and is not suitable for multilayer ceramic capacitor that needs a material that has true giant electric permittivity. In order to continue to respond to market needs, we need to increase the number of layers of the existing type of capacitors by using BT. At the same time, we will have to make further efforts to find materials that can truly improve the performance of multilayer ceramic capacitors.

Our experiments revealed that BT with SiO_2 coating sintered by the spark plasma sintering method shows expressions of apparent giant electric permittivity. But we also observed that after polishing the disk surface, the specific resistance dropped to as low as $10^8\ \Omega\cdot$cm. These results led us to find that the spark plasma sintered BT500@Si5 disk that is mentioned in Chung's report is an isolated surface semiconductor ceramic capacitor. Capacitors of simple internal barrier layer capacitor type and isolated surface semiconductor type cannot be used for multilayer ceramic capacitors that have a multilayer thin film structure because there is a trade-off between varistor voltage and relative permittivity. Efforts for thinning dielectric layers are approaching the limit. In order to circumvent this situation, we need to find a material that has a truly gigantic relative permittivity.

[1]G. Arlt, D. Hennings, and G. de With, J. Appl. Phys. **58**, 1619 (1985).
[2]T. Tsurumi, H. Adachi, H. Kakemoto, S. Wada, Y. Mizuno, H. Chazono, and H. Kishi, Jpn. J. Appl. Phys., Part 1 **41**, 6929 (2002).
[3]A. P. Ramirez, M. A. Subramanian, M. Gardel, G. Blumberg, D. Li, T. Vogt, and S. M. Shapiro, Solid State Commun. **115**, 217 (2000).
[4]M. A. Subramanian, D. Li, N. Duan, B. A. Reisner, and A. W. Sleight, J. Solid State Chem. **151**, 323 (2000).
[5]U.-C. Chung, C. Elissalde, S. Mornet, M. Maglione, and C. Estournes, Appl. Phys. Lett. **94**, 072903 (2009).
[6]A. Artemenko, C. Elissalde, U.-C. Chung, C. Estournes, S. Mornet, I. Bykov, and M. Magline, Appl. Phys. Lett. **97**, 132901 (2010).
[7]U.-C. Chung, C. Elissalde, F. Mompiou, J. Majimel, S. Gomez, C. Estournes, S. Marinel, A. Klein, F. Weill, D. Michau, S. Mornet, and M. Maglione, J. Am. Ceram. Soc. **93**, 865 (2010).
[8]S. Mornet, C. Elissalde, V. Hornebecq, O. Bidault, E. Duguet, A. Brisson, and M. Maglione, Chem. Mater. **17**, 4530 (2005).
[9]K. Mukae, Ceram. Jpn. **38**(12), 973 (2003).